directions. After forming the memory element, the Y address lines **50** are built on the memory elements. Although not shown here, as conventional memories, some circuits need to be accomplished before and after fabricating memory elements to isolate the each memory element for reading and writing.

WHAT IS CLAIM IS:

1. A method of fabricating extra-small openings comprising the steps of:

a. forming a composite-phase thin film layer where one phase forms extra-small particles and embedded in another phase which forms a matrix layer;

b. removing the phase which forms the extra-small particles.

2. The thickness of the composite-phase thin film in claim **1** is in the range of about 1 to 100 nm.

3. The size of the said extra-small particle is in the range of about 1 to 100 nm.

4. The volume ratio of the said nano-dot particle phase and the said matrix layer is in the range of about 3:1 to 1:200.

5. The materials of two phases in claim **1** are not mixable.
6. The material of the phase in claim **1** which forms ultra-small particles is active to some chemical, while another phase in claim 1 which forms matrix layer is inactive to the chemical.
7. The materials of the phase in claim **1** which form matrix layer is one or more materials selected from the oxide, nitride, boride, carbide, boron, silicon, carbon, carboxynitride and mixture thereof.
8. A phase-change memory device comprising:

a. a pair of electrodes; and

b. a resistive layer with a plurality of ultra-small resistive element, or

c. a lamination of said resistive layer and conductive layer.

9. The extra-small resistive element in claim **8** is formed by filling the phase-change resistive element material in the opening formed by the method of claim **1**.
10. The top surface and bottom surface of the said resistive elements in claim **8** contacts directly with the top and bottom electrodes, respectively.
11. The device in claim **8** with lamination of resistive layer and conductive layer wherein the top surface and

bottom surface contact with said adjacent conductor layer.

12. The device of claim **8** wherein the resistive layer has a thickness in the range of about 1.0 to 100 nm.

13. The device of claim **8** wherein the size of the resistive element is in the range of about 1.0-100 nm in diameter.

14. The device of claim **8** wherein the material of electrode layer and the conductive layer in the lamination resistive element is selected from the high melting temperature metals, alloys and conductive compounds.

15. The programming of the device of claim **8** includes a pulse current of short duration and higher current and a pulse current with longer duration and lower current.

16. A programming metallization cell memory (PMCm) comprising:

a. a pair of electrodes; and

b. a thin metal layer; and

c. a single resistive layer with a plurality of ultra-small solid electrolyte resistive element, or

d. a lamination of said resistive layer, thin metal layer and conductive layer.

17. The said extra-small solid electrolyte resistive element in claim **16** is formed by filling the solid electrolyte resistive element material in the opening formed by the method of claim **1**.

18. The top surface and bottom surface of the said solid electrolyte resistive elements in the claim **16** contact directly with the adjacent metal layer and bottom electrode, respectively.

19. The device of claim **16** with lamination of resistive layer, thin metal layer and conductive layer wherein the top surface and bottom surface of said solid electrolyte element contact with adjacent said conductor layer and thin metal layer.

20. The device of claim **16** wherein the size of the solid electrolyte resistive element is in the range of about 1.0-100 nm in diameter.